Remarks

Claims 1-2 are pending in the application. Claims 1-2 are rejected. Claims 1 and 2 are amended herein. The Abstract is objected to. All rejections and objections are respectfully traversed.

The Abstract of the Disclosure is objected to. A substitute Abstract of the Disclosure, which will replace any previous version of the Abstract of the Disclosure, is submitted herewith as "Appendix A."

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Buchanan et al., (U.S. 6,970,435 – Buchanan).

The invention generates lesser width parallel data words from a greater width parallel data word by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words. Buchanan describes partitioning a 16 bit data stream into four groups of four bit nibbles, see col. 4, lines 50-66, below:

interface is on a byte (8-bit) boundary. According to the present invention, it is more advantageous to partition the bits into nibbles for processing and sending through the serial link. In one embodiment of the present invention, 16-bit parallel data streams are supplied to DASL interface. The bit streams are partitioned into four groups of four bit (4 bits=1 nibble) streams. Each of the nibbles is processed according to the teaching of the present invention and is sent over a serial link. As a consequence, to transmit the 16-bit, four serial links would be required. Each nibble of data is processed in the same way; therefore, the description of one (set forth hereinafter) is intended to cover the processing of the others. The four parallel data bit streams are transformed into a high speed serial bit stream by latching each of the four bit streams in one of the Latch L1 through L4 and sequentially strobing the latched information at four time the parallel clock rate using Multiplexer Circuit 22. The data

Therefore, Buchanan teaches partitioning a 16 bit parallel data word into 4 bit nibbles using one of latches L1-L4 for each nibble, and then sequentially strobing the latched nibbles using the multiplexer circuit 22.

In contrast, the invention generates lesser width parallel data words by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words. Then, the lesser width parallel data words are serialized and transmitted. The Examiner is requested to specifically point out where Buchanan teaches "interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words' as claimed.

The Examiner has erroneously applied the same section of Buchanan, i.e., col. 4, lines 62-64, to teach both the step of generating lesser width parallel data words and the step of serializing. A person of ordinary skill in the art would readily understand that Buchanan describes partitioning to generate lesser width words at col. 4, lines 54-56, and describes serializing at col. 4, lines 62-64. There is no teaching of interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words, as claimed.

Further, col. 5, lines 18 -21 explicitly teaches serializing data, not generating lesser width data words as asserted by the Examiner.

circuit. As stated previously, the function of the transmitter circuit is to serialize nibbles of data onto separate serial streams that are transmitted on separate serial links. The nibble of data is selected from parallel bit streams. Four latches labelled L0, L1, L2 and L3 receive data labelled DATAIN0, DATAIN1, DATAIN2 and DATAIN3. The data are from parallel bit streams. Each of the latches comprises

underlining added

Therefore, it should be understood that the section referenced by the Examiner to teach generating lesser width data words is actually used explicitly to describe serializing in the reference. Therefore, the cited section is useless for teaching generating lesser width parallel data words, as claimed. Therefore, the Examiner is requested to reconsider and withdraw the rejections based on Buchanan.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan in view of Nishida, et al., (U.S. 5,978,486 – "Nishida").

As stated above with respect to claim 1, Buchanan fails to teach lesser width parallel data words generated from a greater width parallel data word as claimed.

Nishida is referenced to teach scrambling the data in the lesser width parallel data words. Nishida teaches a scrambling parallel data, see e.g. col. 18, lines 33-39, below:

A fourth embodiment of the present invention relates to a data scrambling apparatus that receives information data to be scrambled, by 8 bits in parallel and outputs scrambled data by 8 bits in parallel. FIG. 7 shows an example of the data scrambling apparatus. In order to facilitate and embody the explanation, a generating polynomial, $G(X)=1+X^{-4}+X^{-9}$, is employed.

Scrambling data, including parallel data, is known. What Nishida, alone or in combination with Buchanan, fails to make obvious is scrambling lesser width parallel data words concurrently generated from a greater width

parallel data word 'by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words' as claimed. At best, the proposed combination might teach scrambling ***partitioned*** parallel data words, but can never teach or suggest what is claimed.

Further, there is no motivation to combine Buchanan with Nishida in either reference. The Examiner's alleged motivation to combine the references, and his supportive reference to Buchanan at col. 1, lines 26-29, is non-sequitor.

It is believed that this application is now in condition for allowance. A notice to this effect is respectfully requested. Should further questions arise concerning this application, the Examiner is invited to call Applicant's attorney at the number listed below.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 50-3650.

Respectfully submitted,
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